Electronic Version
Stylesheet Version v1.1.1

NONVOLATILE SEMICONDUCTOR MEMORY DEVICE HAVING DIVIDED BIT LINES

Abstract

A non-volatile semiconductor memory device having divided bit lines. A main bit line is controlled by at least one bit line selection device to transfer its potential to a selected sub bit line, such that memory cells in a selected sector work and overloading of the bit line generated by a parasitic capacitance can be prevented. The memory cells and the bit line selection device are arranged in parallel in a P-well and a N-well, respectively, thereby preventing disturbances during programming or erasing the bit line.